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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/593,891	06/14/2000	Sadao Nakayama	NFC DP-624	8215

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/593,891	NAKAYAMA, SADAO	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 9 and 11 - 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9, 11 and 13* is/are allowed.

6)☒ Claim(s) *1 - 8, 12, and 14 - 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. §.119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on December 17, 2004 has been received and entered in the case.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation in claims 12 and 14 "wherein said third pad is in direct contact with said second pad" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will

be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 14 is objected to because of the following informalities:

(A) Claim 14 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim, or amend the claim to place the claim in proper dependent form, or rewrite the claim in independent form. For example, "a package substrate" in line 3 of the claim 14 should be -- the package substrate --.

- line 3, "a package substrate" lacks antecedent basis;
- line 4, "a first chip" lacks antecedent basis;
- line 5, "a wiring substrate" lacks antecedent basis; and
- line 9, "a second chip" lacks antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 12 and 14 – 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Khandros et al. (U.S. Pat. No. 5, 347, 159).

Regarding claim 12, Khandros et al. discloses in e.g., Fig. 11 and column 14, line 56 – column 15, line 43 a semiconductor device, comprising:

- a package substrate (the substrate that supports the element 393) having a first pad (at the connection area that is connected by the wire 395 on the substrate);
- a first chip (393; column 14, line 61) having a second pad (391; column 14, line 60) and formed on said package substrate;
- a wiring substrate (383 that is located at bottom and side surfaces of the chip 320) formed on said first chip, said wiring substrate having a third pad (346), a fourth pad (at the connection area that is connected to the pad 328 by the wire) and a wiring pattern (the wiring circuit on the element 383 that connects between the third pad 346 and fourth pad) connected between said third and fourth pads; and
- a second chip (320; column 14, line 59) having a fifth pad (328) and formed on said wiring substrate,
- wherein said third pad (346) is in direct contact with said second pad (391).

Regarding claim 14, Khandros et al. discloses in e.g., Fig. 11 a semiconductor device, comprising:

- a package substrate (the substrate that supports the element 393) having a plurality of first pads (at the entire connection areas that that connected by the wiring 395s on the substrate);

- a first chip (393) having a plurality of second pads (391) and formed on said package substrate;
- a wiring substrate (383 that is located at bottom and side surfaces of the chip 320) formed on said first chip, said wiring substrate having a plurality of third pads (346), a plurality of fourth pads (at the entire connection areas that are connected to the pad 328s by the wires) and wiring patterns (the wiring circuits on the element 383 that connects between the third pad 346 and fourth pad) connected between said third and fourth pads; and
- a second chip (320) having a plurality of fifth pads (328) and formed on said wiring substrate;
- wherein said third pads (346) are in direct contact with said second pads (391).

Regarding claim 15, Khandros et al. discloses in e.g., Fig. 11 one of said first pads being connected to one of said second pads as well as one of said third pads (electrical connections thru the second pads and wire).

Regarding claim 16, Khandros et al. discloses in e.g., Fig. 11 said wiring substrate (383 that is located at bottom and side surfaces of the chip 320) being a sheet wiring substrate (see Fig. 11).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takiar et al. '398 in view of Rostoker '570.

Regarding claims 1, Takiar et al. discloses in e.g., Fig. 6, Fig. 7 and column 2, lines 49 – 57 a stacked semiconductor storage device (Since Takiar et al. discloses the stacked MCMs is all memory devices, it meets this preamble. Furthermore, this limitation has not been given patentable weight because this preamble merely states the purpose or intended use of the invention rather than any distinct definition of any of the claimed invention's limitations) comprising, in combination,

- a lower chip (136 or/and 158) and an upper chip (140 or/and 162) superimposed on a substrate (142 or/and 156),
- said semiconductor storage device further comprising:
- a wiring substrate (138 or/and 160; column 7, lines 9 – 15) having wiring patterns (at the wiring patterns in Fig. 2 and column 6, lines 36 – 57) thereon, interposed between and in direct contact with both said lower chip and said upper chip, for relaying electric connection (at the 5th pad of the elements 168 from the right-down side) between bonding pads (pads on the element 162) on said upper chip (162) and bonding pads (at the connection area or elements 168) on said substrate (156),
- wherein the bonding pads on said upper chip (162) are arranged in a line running perpendicular (the up-and-down array of pads on the upper chip 162 is perpendicular to the right-to-left array of pads 168 on the substrate 156) to a line of bonding pads (at the right-to-left array of pads 168) on the substrate (156);

- wherein said upper chip (162) has an upper and a lower surface, said lower surface facing said substrate.

However, Takiar et al. does not disclose the bonding pads on said upper chip that connect to the bonding pads of said substrate being disposed on the lower surface of said upper chip. Rostoker teaches in Figs. 1a and 1b bonding pads (108) on a chip that connects to bonding pads (at the connection areas on the elements 112a) of a substrate (110) being disposed on the lower surface of the chip. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Takiar et al. by using the other end of the wiring pattern to connect to the terminal on the surface of the lower chip as taught by Rostoker. The ordinary artisan would have been motivated to modify Takiar et al. in the manner described above for at least the purpose of providing a high I/O semiconductor die (column 3, lines 24 – 35).

Regarding claim 2, Takiar et al. discloses in e.g., Fig. 6, Fig. 7 and column 2, lines 49 – 57 said wiring pattern (160) being connected to a first terminal (at the pads on the element 162) on a surface of the upper chip (162), a second terminal (at the 5th pads from right-down side on the element 160) being connected to a terminal (at the pads 168) on a surface of the substrate (156), and said wiring pattern (160) connecting the second terminal (at the pads on the element 160) to said terminal (pads on the element 162) on a surface of said upper chip (162).

Regarding claim 3, Takiar et al. discloses in e.g., Fig. 6 and Fig. 7 a bonding wire (any wiring bonds in the structure) for connecting said terminal (168) of the surface of said substrate (156) with said second terminal (at the 5th pads from right-down side on the element 160).

Regarding claim 4, Takiar et al. and Rostoker disclose there being provided a wiring pattern (160) whose one end is connected to a terminal on a rear surface of said upper chip, and whose other terminal is (electrically) connected to a terminal on a surface of said lower chip.

Regarding claims 5 and 6, Takiar et al. discloses in e.g., Fig. 6 and Fig. 7 said terminal of the surface of said lower chip (158) being connected to said terminal of the surface of said substrate (156) by a third bonding wire.

Regarding claim 7, Takiar et al. and Rostoker disclose the claimed invention except that the wiring substrate being a board instead of a sheet. Since it is known in the art that a sheet wiring substrate is an equivalent structure of the board wiring substrate. Therefore, because these two "sheet wiring substrate" and "board wiring substrate" were art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute the sheet wiring substrate for the board wiring substrate. The ordinary artisan would have been motivated to modify Takiar et al. in the manner described above for at least the purpose of decreasing height of the package.

Regarding claim 8, Takiar et al. discloses in e.g., Fig. 6 and Fig. 7 said wiring substrate (142 or/and 160) being a board wiring substrate.

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khandros et al.

Khandros et al. discloses the claimed invention except that the wiring substrate being a board instead of a sheet. Since it is known in the art that a sheet wiring substrate is an equivalent structure of the board wiring substrate. Therefore, because these two "sheet wiring substrate" and "board wiring substrate" were art-recognized equivalents at the time the invention was made, one

of ordinary skill in the art would have found it obvious to substitute the sheet wiring substrate for the board wiring substrate. The ordinary artisan would have been motivated to modify Khandros et al. in the manner described above for at least the purpose of decreasing height of the package.

Allowable Subject Matter

9. Claims 9, 11 and 13 are allowed.

10. The following is an examiner's statement of reasons for allowance:

The prior art of record does not teach or suggest, either singularly or in combination, at least the limitation of a first bonding wire connecting a first pad and a third pad and a second bonding wire connecting a fourth pad and a fifth pad when the fourth pad on the wiring substrate is connected to the fifth pad on a second chip while the fourth pad, a third pad and a wiring pattern are formed on a wiring substrate and the fourth pad is connected to a third pad by a wiring pattern.

Response to Arguments

11. Applicant's arguments filed on December 21, 2004 have been fully considered but they are either moot in light of the new grounds of rejection or are not persuasive.

On page 6, fifth paragraph, applicant argues the combination of Takiar et al. and Rostoker is improper as Takiar et al. teaches away from its combination with Rostoker, specifically, that Rostoker teaches flip chip while Takiar et al. teaches away from flip chip. This argument is not persuasive. Applicant should note that disclosed examples and preferred embodiments do not constitute a teaching away from a broader disclosure or nonpreferred

embodiments. In re Susi, 440 F.2d 442, 169 USPQ 423 (CCPA 1971). "A known or obvious composition does not become patentable simply because it has been described as somewhat inferior to some other product for the same use." In re Gurley, 27 F.3d 551, 554, 31 USPQ2d 1130, 1132 (Fed. Cir. 1994). MPEP 2123. In this case, Takiar et al. discloses in e.g., column 7, lines 33 – 39 that some of the elements in the stack may be interconnected by using "flip chip" connection. Also, Takiar et al. discloses in e.g., column 2, lines 58 – 62 that among the advantages of the flip chip are improved thermal performance, electrical characteristics and reworkability. Since Takiar et al. discloses "flip chip" connection, Takiar et al. does not teach away from its combination with Rostoker. Thus, the combination of Takiar et al. and Rostoker is proper.

For the above reason, the rejection is maintained.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Wednesday, March 16, 2005

GEORGE ECKERT
PRIMARY EXAMINER